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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known		
	Application Number	09/866938	
	Filing Date	May 29, 2001	
	First Named Inventor	Noble Jr., Wendell	
	Group Art Unit	2813	
	Examiner Name	Chen, Jack	
Sheet 1 of 1	Attorney Docket No: 303.330US3		

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
///	US-4,920,389	04/24/1990	Itoh, Massahiro	357	23.6	03/07/1989
~/	US-5,363,325	11/08/1994	Sunouchi, K, et al	365	149	07/01/1992
~	US-5,365,477	11/15/1994	Cooper Jr., J A, et al	365	174	06/16/1992
~	US-5,429,955	07/04/1995	Joyner, K. A., et al	437	26	10/26/1992
~	US-5,640,350	06/17/1997	Iga, A.	365	186	08/21/1996
./_	US-5,696,011	12/09/1997	Yamazaki, S. , et al	437	40 TFI	03/23/1993
	US-5,714,793	02/03/1998	Cartagena, E., et al	257	507	08/21/1996
. ~ _	US-5,998,820	12/07/1999	Chi, M , et al	257	296	11/24/1998
$\sim$	US-6,172,535	01/09/2001	Hopkins, M.	327	66	11/04/1999
~	US-6,181,121	01/30/2001	Kirkland,, et al			
7	US-6,181,196	01/30/2001	Nguyen, B.	327	539	12/14/1998
~	US-6,323,719	11/27/2001	Chang, C., et al	327	478	05/08/2000

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>

OTHER DOCUMENTS NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T	
~		RHYNE, In: Fundamentals of Digital Systems Design, Prentice Hall, New Jersey,(1973),pg. 70-71		
		SU, D., et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", <u>IEEE Journal of Solid State Circuits</u> , <u>28(4)</u> , (1993),pp. 420-430		

EXAMINER

Sarbell

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4/18/03